

What is claimed is:

1. A method of forming a  $\text{SiO}_x\text{N}_y$  gate dielectric, comprising:  
providing a structure comprising a silicon oxide film formed on a silicon substrate;  
heating the structure in an atmosphere comprising  $\text{NH}_3$  to incorporate nitrogen into the silicon oxide film; and then  
exposing the structure to a plasma comprising a nitrogen source to form a  $\text{SiO}_x\text{N}_y$  gate dielectric on the substrate.
2. The method of claim 1, further comprising annealing the structure after the exposing the structure to the plasma.
3. The method of claim 2, wherein the annealing is performed in an atmosphere comprising  $\text{O}_2$ .
4. The method of claim 3, wherein the annealing further comprises annealing the structure in an inert or reducing atmosphere before the annealing in an atmosphere comprising  $\text{O}_2$ .
5. The method of claim 1, wherein the nitrogen source is selected from the group consisting of  $\text{N}_2$ ,  $\text{NH}_3$ , and combinations thereof.
6. The method of claim 1, wherein heating the structure comprises heating the structure to a temperature of at least about  $700^\circ\text{C}$  at a pressure of less than about 100 Torr.
7. The method of claim 1, wherein exposing the structure to a plasma is performed at a pressure of between about 1 mTorr and about 30 mTorr.

PATENT

Attorney Docket No.: AMAT/8629/FEP/GCM/RKK

Express Mail No.:EV335470144US

8. The method of claim 1, further comprising forming the silicon oxide film by oxidizing a top surface of the silicon substrate.
9. The method of claim 1, wherein substantially no oxygen is incorporated into the structure while heating the structure in an atmosphere comprising  $\text{NH}_3$ .
10. A method of forming a  $\text{SiO}_x\text{N}_y$  gate dielectric in an integrated processing system, comprising:
  - heating a structure comprising a silicon oxide film formed on a silicon substrate in an atmosphere comprising  $\text{NH}_3$  in a first processing chamber of the integrated processing system to incorporate nitrogen into the silicon oxide film;
  - transferring the structure to a second processing chamber of the integrated processing system; and then
  - exposing the structure to a plasma comprising a nitrogen source in the second processing chamber to form a  $\text{SiO}_x\text{N}_y$  gate dielectric on the substrate.
11. The method of claim 10, further comprising:
  - transferring the structure to a third processing chamber of the integrated processing system; and
  - annealing the substrate in the third processing chamber.
12. The method of claim 11, further comprising:
  - introducing the silicon substrate into the integrated processing system; and
  - forming the silicon oxide film on the substrate in the third processing chamber of the integrated processing system to form the structure comprising a silicon oxide film on a silicon substrate.
13. The method of claim 12, further comprising:
  - transferring the structure to a fourth processing chamber of the integrated processing system after the annealing the substrate; and

PATENT

Attorney Docket No.: AMAT/8629/FEP/GCM/RKK

Express Mail No.:EV335470144US

depositing a polysilicon layer on the  $\text{SiO}_x\text{N}_y$  gate dielectric in the fifth processing chamber.

14. The method of claim 11, further comprising:

introducing the silicon substrate into the integrated processing system; and  
forming the silicon oxide film on the substrate in a fourth processing chamber of the integrated processing system to form the structure comprising a silicon oxide film on a silicon substrate.

15. The method of claim 14, further comprising:

transferring the structure to a fifth processing chamber external to the integrated processing system after the exposing the structure to the plasma; and  
depositing a polysilicon layer on the  $\text{SiO}_x\text{N}_y$  gate dielectric in the fifth processing chamber.

16. The method of claim 11, wherein the annealing is performed in an atmosphere comprising  $\text{O}_2$ .

17. The method of claim 16, wherein the annealing further comprises annealing the structure in an inert or reducing atmosphere before the annealing in an atmosphere comprising  $\text{O}_2$ .

18. The method of claim 10, further comprising transferring the structure to a cool down chamber after the heating and before the transferring the structure to a second processing chamber.

19. A  $\text{SiO}_x\text{N}_y$  gate dielectric, formed by a method comprising:

heating a structure comprising a silicon oxide film formed on a silicon substrate in an atmosphere comprising  $\text{NH}_3$  to incorporate nitrogen into the silicon oxide film; and then

exposing the structure to a plasma comprising a nitrogen source to form a  $\text{SiO}_x\text{N}_y$  gate dielectric on the substrate.

20. The  $\text{SiO}_x\text{N}_y$  gate dielectric of claim 19, wherein the gate dielectric comprises at least 5% nitrogen.

21. The  $\text{SiO}_x\text{N}_y$  gate dielectric of claim 19, wherein the method further comprises annealing the structure after the exposing the structure to a plasma.

22. The  $\text{SiO}_x\text{N}_y$  gate dielectric of claim 19, wherein substantially no oxygen is incorporated into the structure while heating the structure in an atmosphere comprising  $\text{NH}_3$ .

23. The  $\text{SiO}_x\text{N}_y$  gate dielectric of claim 19, wherein the nitrogen source is selected from the group consisting of  $\text{N}_2$ ,  $\text{NH}_3$ , and combinations thereof.

24. The  $\text{SiO}_x\text{N}_y$  gate dielectric of claim 19, wherein the method further comprises forming the silicon oxide film by oxidizing a top surface of the silicon substrate.

25. The  $\text{SiO}_x\text{N}_y$  gate dielectric of claim 19, wherein the method further comprises placing the silicon substrate in an integrated processing system and not removing the structure from the integrated processing system until after the gate dielectric is formed.

26. The  $\text{SiO}_x\text{N}_y$  gate dielectric of claim 25, wherein the method further comprises depositing a polysilicon layer on the substrate, wherein the structure is not removed from the integrated processing system until after the polysilicon layer is deposited.